

ABSTRACT OF THE DISCLOSURE

A failure detection system includes a wafer test information input unit which acquires pass/fail maps for wafers for a plurality of types of semiconductor devices, displaying failure chip areas based on results of electrical tests performed on chips; an analogous test information input unit which classifies the electrical tests into analogous electrical tests with regard to analogous failures among the semiconductor devices; a subarea setting unit which assigns subareas common to the types of semiconductor devices on a wafer surface; a characteristic quantity calculation unit which statistically calculates characteristic quantities based on a number of the failure chip areas included in the subareas for each analogous electrical test; and a categorization unit which obtains correlation coefficients between the characteristic quantities corresponding to the subareas, and classifies clustering failure patterns of the failure chip areas into categories by comparing the correlation coefficients with a threshold.